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Martin, D.E.; Wilsey, P.A.; Hoekstra, R.J.; Keiter, E.R.; Hutchinson, S.A.; Russo, T.V.; Waters, L.J.;
Simulation Symposium, 2004. Proceedings. 37th Annual
18-22 April 2004 Page(s):231 - 237
Digital Object Identifier 10.1109/SIMSYM.2004.1299487

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☐ **2. A multimodel approach to reasoning and simulation**
Fishwick, P.A.; Narayanan, N.H.; Sticklen, J.; Bonarini, A.;
Systems, Man and Cybernetics, IEEE Transactions on
Volume 24, Issue 10, Oct. 1994 Page(s):1433 - 1449
Digital Object Identifier 10.1109/21.310527

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Sungjoo Yoo; Jong-Eun Lee; Jinyong Jung; Kyungseok Rha; Youngchul Cho; Kiyoung Choi;
Design, Automation and Test in Europe Conference and Exhibition 2000, Proceedings
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Digital Object Identifier 10.1109/DATE.2000.840857
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☐ 2. **Combined data-driven and event-driven scheduling technique for fast distributed cosimulation**
Dohyung Kim; Chan-Eun Rhee; Soonhoi Ha;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 10, Issue 5, Oct. 2002 Page(s):672 - 678
Digital Object Identifier 10.1109/TVLSI.2002.801572
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☐ 3. **Fast and Accurate Cosimulation of MPSoC Using Trace-Driven Virtual Synchronization**
Youngmin Yi; Dohyung Kim; Soonhoi Ha;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 26, Issue 12, Dec. 2007 Page(s):2186 - 2200
Digital Object Identifier 10.1109/TCAD.2007.907048
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☐ 4. **Virtual synchronization technique with OS modeling for fast and time-accurate cosimulation**
Youngmin Yi; Dohyung Kim; Soonhoi Ha;
Hardware/Software Codesign and System Synthesis, 2003. First IEEE/ACM/IFIP International Conference on
1-3 Oct. 2003 Page(s):1 - 6
AbstractPlus | Full Text: PDF(527 KB) IEEE CNF
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5. **Performance improvement of multi-processor systems cosimulation based on SW analysis**
Jinyong Jung; Sungjoo Yoo; Kiyoung Choi;
<u>Design, Automation and Test in Europe, 2001. Conference and Exhibition 2001. Proceedings</u>
13-16 March 2001 Page(s):749 - 753
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☐ 2. **IEEE Standard for the Functional Verification Language e**
Aug. 3 2008 Page(s):c1 - 464
Digital Object Identifier 10.1109/IEEESTD.2008.4586409
AbstractPlus | Full Text: PDF(4230 KB)   IEEE STD

☐ 3. **Draft Standard for the Functional Verification Language 'e'**
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☐ 4. **IEEE standard Verilog hardware description language**
2001 Page(s):0_1 - 856
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☐ 5. **IEEE standard hardware description language based on the Verilog(R) hardware description language**
14 Oct. 1996
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☐ 6. **Unapproved IEEE Draft Standard for the Functional Verification Language 'e' (Replaced by the approved draft)**
2005
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☐ 7. **IEEE Unapproved Draft Standard for Verilog? Hardware Description Language (Revision of 1364-1995) Replaced by approved draft**
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8. **IEEE Approved Draft Standard for Verilog? Hardware Description Language Superseded by 1364-2005**
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9. **IEEE Standard for the Functional Verification Language 'e'**
2006 Page(s):0_1 - 371

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10. IEEE Std 1364 -2005 IEEE Standard for Verilog Hardware Description Language
2006 Page(s):0_1 - 560

AbstractPlus | Full Text: PDF(5970 KB)   IEEE STD

11. **Behavioural languages - Part 4: Verilog hardware description language**
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12. **Fast and Accurate Cosimulation of MPSoC Using Trace-Driven Virtual Synchronization**
Youngmin Yi; Dohyung Kim; Soonhoi Ha;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 26, Issue 12, Dec. 2007 Page(s):2186 - 2200
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13. **Timed compiled-code functional simulation of embedded software for performance analysis of SOC design**
Jong-Yeol Lee; In-Cheol Park;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
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